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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/054,173

01/18/2002

Brian J. Malone

01-1008-A

4542

7590

01/25/2006

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EXAMINER

CHOI, JACOB Y

ART UNIT

PAPER NUMBER

2875

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EP

Office Action Summary	Application No. 10/054,173	Applicant(s) MALONE ET AL.	
	Examiner Jacob Y. Choi	Art Unit 2875	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6, 8-10, 12-23, 25, 26, & 28-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-10, 12-23, 25, 26 and 28-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01/18/2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. Any structural detail that is of sufficient importance to be described should be shown in the drawing (Ex parte Good, 1911 C.D. 43, 164 O.G. 739 (Comm'r Pat. 1911).) See MPEP 608.02. Therefore, applicant needs to show a plurality of compartments, each compartment being generally concave, the conductive material and reflective coating are formed on the substrate within the same vacuum chamber, & the conductive material and reflective coating are formed on the substrate simultaneously in the same vacuum chamber.

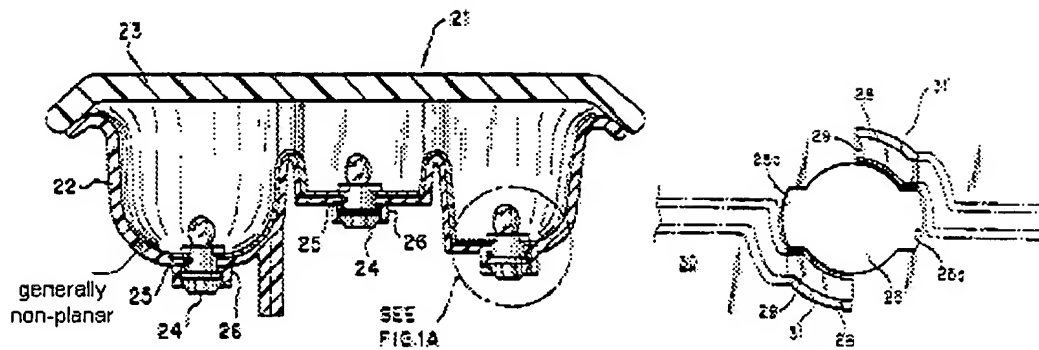
Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

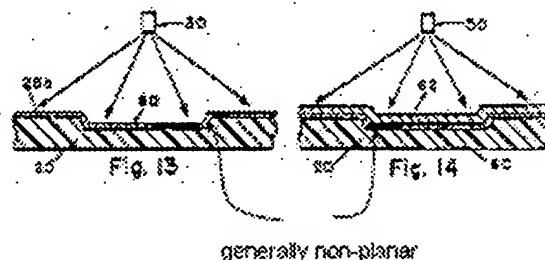
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 8-10, 12-20, 22, 23, 25, 26 & 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (USPN 6,290,380) in view of Elarde (USOPN 4,532,152).

Regarding claims 1, Suzuki et al. discloses the printed circuit board being utilized for a vehicle lamp housing and the conductive material (e.g., 29) is connected to at least one or more light source(s) (e.g., 37) and its power source(s) (e.g., Figures 11-12).



Elarde teaches a method of manufacturing a printed circuit board comprising a depositing particles by direct metallization to form a layer of conductive material on a contoured/generally non-planar surface of a substrate that forms part of the circuit board, in order to form part of one or more electrical spray circuits (claim 1, 14, & 15).



Suzuki et al. discloses the claimed invention except for the various well-known methods of depositing particles to form a layer of conductive material on a substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize well known method of manufacturing a printed circuit board on a substrate/other suitable high temperature plastics (e.g., column 9, 60-65 of Elarde) on the lamp housing as taught by Suzuki et al. in order to provide conductive circuitry and connection to the light source(s) and its power source(s).

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Note: claims in a pending application should be given their broadest reasonable interpretation. *In re Pearson*, 181 USPQ 641 (CCPA 1974).

“generally non-planar” - not lying in one plane

Regarding claim 8, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Elarde discloses a step of forming distinct electrical pathways in the layer of conductive material during deposition.

Regarding claim 9, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Elarde discloses the distinct electrical pathways are formed (e.g., “coat of brass, thin brass plus electro less copper, or electro less copper plus electroplated copper”) by masking the lamp housing prior to deposition of the layer of conductive material on the lamp housing.

Regarding claim 10, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. discloses depositing a reflective coating on the substrate (e.g., 30).

Regarding claim 12, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Elarde discloses a step of applying a spray seal on the substrate (additional layer; figures 14, 15, 18, 19, 21, 22).

Regarding claim 13, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Elarde discloses a step of applying a protective coating to the conductive material (e.g., “additional layer”; figures 14, 15, 18, 19, 21, 22).

Regarding claim 14, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Elarde discloses the step of depositing a conductive layer further comprises depositing one or more terminals.

Regarding claim 15, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Elarde discloses the step of depositing a conductive further layer comprises a depositing at least one connection for electrically connecting the conductive layer.

Regarding claim 16, Suzuki et al. clearly discloses a conductive layer (e.g., figure 4) for one or more electrical circuits deposited directly (e.g., figure 3) on the substrate.

Suzuki et al. discloses the claimed invention except for the conductive layer is 1 to 4 microns thick.

Elarde teaches that the depth of the conductive layer is approximately 0.003-0.010. It would have been obvious to one having ordinary skill in the art at the time the invention was made to specify workable range of the conductive layer on the substrate, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Note: it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson*, 136 USPQ 184.

Regarding claim 17, Suzuki et al. in view of Elarde discloses the claimed invention, explained above.

The method of forming the device is not germane to the issue of patentability of the device itself. Therefore, this (e.g., "conductive layer is formed by vacuum deposition of the electrical circuits on the substrate") limitation has not been given patentable weight.

Regarding claim 18, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose the conductive layer is directly embedded in the substrate.

Regarding claim 19, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose one or more openings in the lamp housing (e.g., 21) for one or more light sources (e.g., 24).

Regarding claim 20, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose one or more terminals attached to the conductive layer at the openings.

Regarding claim 22, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose the light source comprise one or more incandescent lamps (e.g., 24).

Regarding claim 23, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose further comprising a reflective coating (e.g., 30).

Regarding claim 25, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose further comprising a seal (e.g., column 5, lines 30-40).

Regarding claim 26, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose further comprising a protective coating (e.g., reflective coating and other) on the conductive layer.

Regarding claim 28, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose further comprising a single connection for electrically connecting the circuits to one or more power sources (e.g., Figures 1, 6, 11).

Regarding claim 29, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose the housing comprises one or more molded channels (e.g., figures 3, 8-10) to facilitate receipt of the conductive layer.

Regarding claim 30, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose the housing comprises one or more smooth corners to facilitate receipt of the conductive layer.

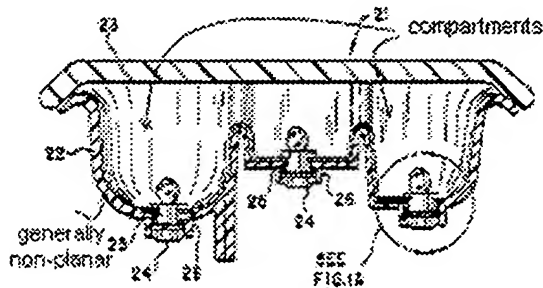
Regarding claim 31, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose the lamp housing is comprised of a thermoplastic material (e.g., column 5, lines 55-65; "*a synthetic resin material*")

Note: it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design variation. *In re Leashin*, 125 USPQ 416.

Regarding claim 32, Suzuki et al. in view of Elarde discloses the claimed invention, explained above. In addition, Suzuki et al. disclose generally non-planar

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surface is comprised of plurality of compartments, each compartment being generally concave.



4. Claims 2-5, 21 & 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (USPN 6,290,380) in view of Elarde (USOPN 4,532,152) as applied to claim 1 above, and further in view of applicant's admitted prior art.

Regarding claims 2-5 & 33-34, Suzuki et al. in view of Elarde discloses the claimed invention, Elarde discloses the direct metallization deposition of the layer of conductive material is deposited by vacuum deposition in a vacuum chamber (*"flame spraying, a combination of electro less plating, electroplating, gas plating"*).

Elarde does not specifically teach other depositing methods on the layer of conductive material.

However, on page 6-7, originally filed applicant's specification states that "spray circuit is applied to inner surface of housing by *one of various known methods* of vacuum deposition ... the LEDs are then soldered in place using *known methods* such as convection reflow ... etc".

It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize well-known methods of depositing the layers of conductive or reflective material for an easier manufacturing process.

Regarding claim 21, Suzuki et al. in view of Elarde discloses the claimed invention except for the light sources comprise one or more light emitting diodes.

On page 6-7, originally filed applicant's specification suggests that "spray circuit is applied to inner surface of housing by *one of various known methods* of vacuum deposition ... the LEDs are then soldered in place using *known methods* such as convection reflow ... etc".

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilized LEDs rather than incandescent lamps, since the examiner takes Official Notice of the equivalence of LEDs and incandescent lamps for their use in the vehicle lamp and the selection of any of these known equivalents would be within the level of ordinary skill in the art.

Response to Amendment

5. Examiner acknowledges that the applicant has amended claim 1, to further limit the claim as "generally non-planar" by replacing the word "contoured". Claim 6 is amended, correctly depending on claim 1. Claims 1-6, 8-10, 12-23, 25, 26 & 28-34 are remaining in the application.

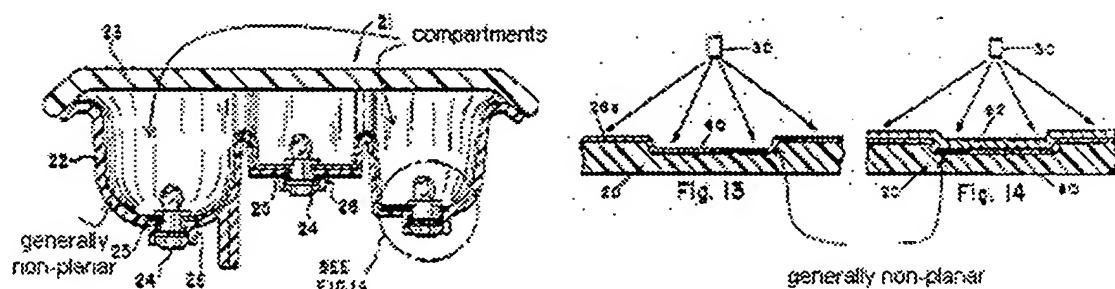
Response to Arguments

6. Applicant's arguments, see pages 7-8, filed 5/24/2005, with respect to claims 31-34 have been fully considered and are persuasive. The claim rejections - 35 USC § 112 of 11/24/2004 has been withdrawn.

7. Applicant's other remaining arguments filed 5/24/2005, see pages 8-11, have been fully considered but they are not persuasive.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the prior art references, Suzuki et al. (USPN 6,290,380) and Elarde (USOPN 4,532,152) clearly shows applying a coating material(s) on a surface that is "generally non-planar" & compartments as indicated below.



In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize well known method of manufacturing a printed circuit board on a substrate/other suitable high temperature plastics (e.g., column 9, 60-65 of Elarde) on the lamp housing as taught by Suzuki et al. in order to provide conductive circuitry and connection to the light source(s) and its power source(s).

Note: claims in a pending application should be given their broadest reasonable interpretation. *In re Pearson*, 181 USPQ 641 (CCPA 1974).

"generally non-planar" - not lying in one plane

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the criticality of follow feature(s) (i.e., conductive layer is 1-4 microns thick) are not demonstrated in the originally filed specification. When relative terms are used in claims wherein the improvement over the prior art rests entirely upon size or weight of an element in a combination of elements, the adequacy of the disclosure of a standard is of greater criticality. The examiner has applied the case law (*In re Aller*, 105 USPQ 233) consistently to the application and the facts in a prior legal decision are sufficiently similar to those in an application under examination. Therefore, it is proper for the examiner to apply the case law considering all the relevant facts.

Note: burden is now on the applicant demonstrating the criticality of the specific limitation.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

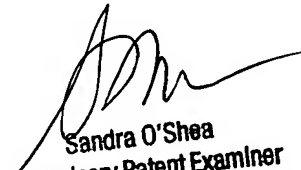
mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Y. Choi whose telephone number is (571) 272-2367. The examiner can normally be reached on Monday-Friday (10:00-7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sandra O'Shea can be reached on (571) 272-2378. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JC



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